Please amend the claims as follows:

B1

1. (Twice amended) A method for developing a fully functional transparent memory module [modules using] comprising an assembly of selected independent primary and backup memory parts,
the method comprising the steps of:
testing a plurality of independent memory [the] parts for failed I/O data line segments;
sorting the parts according to the results of the testing;
identifying failed and working I/O data line segments in [selected] the sorted parts;
selecting at least one primary part having at least one I/O data line failure, and at least one different partially defective backup memory part from said sorted parts; and
combining [the] working I/O data line segments of different selected memory parts, including at least one working I/O data line segment of at least one partially defective backup memory part and working I/O data line segments of a primary part to form a fully functional transparent memory module.

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8. (Twice amended) A method for developing effective chip-on-board memory modules [using] comprising an assembly of a selected combination of independent partially defective memory chips [parts and good memory parts],
comprising the steps of:
assembling the selected chips [parts] as primary chips [parts] and backup chips [parts] onto a chip-on-board memory module assembly;
testing the assembled module for failed I/O data lines in the chips [parts];
identifying [the] operating I/O data line segments in the chips [parts, including operating segments in at least one of the partially defective memory parts]; and
combining [the] identified working I/O data line segments of a partially defective primary chip [part] with a required number of working I/O data line segments of backup memory chips [parts to form an effective fully functional transparent memory module].

B3

12. (Twice amended) A ~~process~~ method for patching selected partially defective independent primary memory parts with selected different partially defective independent backup memory parts to form a memory module functionally transparent to the user, comprising the steps of:
testing the primary memory parts and the backup memory parts before mounting the parts on a board to;
identify operating and failed I/O data line segments of the primary parts and of the backup memory parts;
determining which operating I/O data lines from the backup memory parts to use for selectively patching [the] failed I/O data lines segments of the primary memory parts; and
substituting said determined operating I/O data lines from the backup parts for failed I/O data lines in [the failed segments of] one or more primary parts to form a completed memory module.

Claim 33, line 8, after "parts" and before ";" delete "parts".

50. (Twice amended) A ~~process~~ method for selecting and assembling primary parts and backup parts on a chip-on-board module assembly comprising patterns of solder dot locations for the primary and backup parts, the process comprising the steps of:

performing a wafer test on a memory die;

selecting, as primary parts, partially defective dies that have a reasonable probability of being patched successfully;

selecting, as backup parts, other partially defective dies that test to be suitable for patching [for assembly on a PC module];

assembling the selected primary and backup parts on the PC module;

applying a plastic over coating to the assembled parts; and

[test] testing the module using a chip test applied at the module pins; and

patching failed segments of the primary parts with working segments of the backup parts.

51. (Twice amended) [The process of claim 50, further comprising the steps of:]

A ~~process~~ method for selecting and assembling primary parts and backup parts on a chip-on-board module assembly comprising patterns of solder dot locations for the primary and backup parts,

the process comprising the steps of:

performing a wafer test on a memory die;

selecting, as primary parts, dies that have a reasonable probability of being patched successfully;

selecting, as backup parts, other dies for assembly on a PC module;

assembling the selected primary and backup parts on the PC module;

applying a plastic over coating to the assembled parts; and

test the module using a chip test applied at the module ~~pins~~ pins;

assigning a bar code to the module to identify failed bits;

fill in the solder-dot locations of the primary parts, the solder-dot locations of the back-up parts are left open;

test the module on a full function circuit tester, wherein failed bits are noted, and the module is assigned a bar-code identifying the failed bits;

generate patching instruction charts for the module, wherein the development of the patching instruction charts includes an optimization pass designed to maximize use of smaller patch parts, leaving the larger parts available for patching later-discovered failures;

disconnect solder-dot connections on the primary parts to isolate any failed line;

fill the solder-dot connections to patch in substitute lines, the solder-dot connections selected as identified in the patching instruction charts;

re-test the module, including high temperature stress testing of the module.

Cancel claims 65 and 66.

65
67. (Once amended) [A memory module in accordance with claim 66 wherein:] A memory module comprising:

primary part memory means for storing data;

independent backup part memory means for storing data;

connection means for selectively substituting an operational I/O data line of said backup memory means for a failed I/O data line of said primary memory means;

said memory module has a target memory capacity X,

said primary part memory means has a memory capacity X minus the capacity of any defective I/O data lines therein; and

said independent backup part memory means has available memory capacity at least equal to the capacity of said defective I/O data lines.

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66 (Amended) 65
68. A memory module in accordance with claim [66] 67 wherein:

said connection means comprises a pattern of solder dot connections.

67 (Amended) 65
69. A memory module in accordance with claim [66] 67 wherein:

said connection means comprises a pattern of jumper wire connections.

68 (Amended) 65
70. A memory module in accordance with claim [66] 67 wherein:

said primary part memory means comprise 1MX16 parts; and

said backup part memory means comprise 1MX4 parts.

71
74. (Once amended) [The method of claim 71 further comprising:] A method for constructing a fully functional memory module which utilizes partially defective independent memory circuit parts comprising:

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(a) testing and classifying memory parts in a set of defined classifications

(b) selecting a primary memory part having a selected classification;

(c) selecting a backup memory part having a selected different classification; ~~and~~

(d) constructing a memory module wherein: any defective data lines of the selected primary memory part are replaced by operational data lines of the backup circuit ~~structure~~ structure;

(e) testing said so constructed module as to its operational status to approve use of said module or to identify any operating problem in said module; ~~and~~

(f) reconstructing said module to remove any identified operating problem;

(g) testing said module as to its operational status to approve use as reconstructed or to identify any operating problems; and

(j) repeating steps (h) and (i) as required until the module is approved for service.